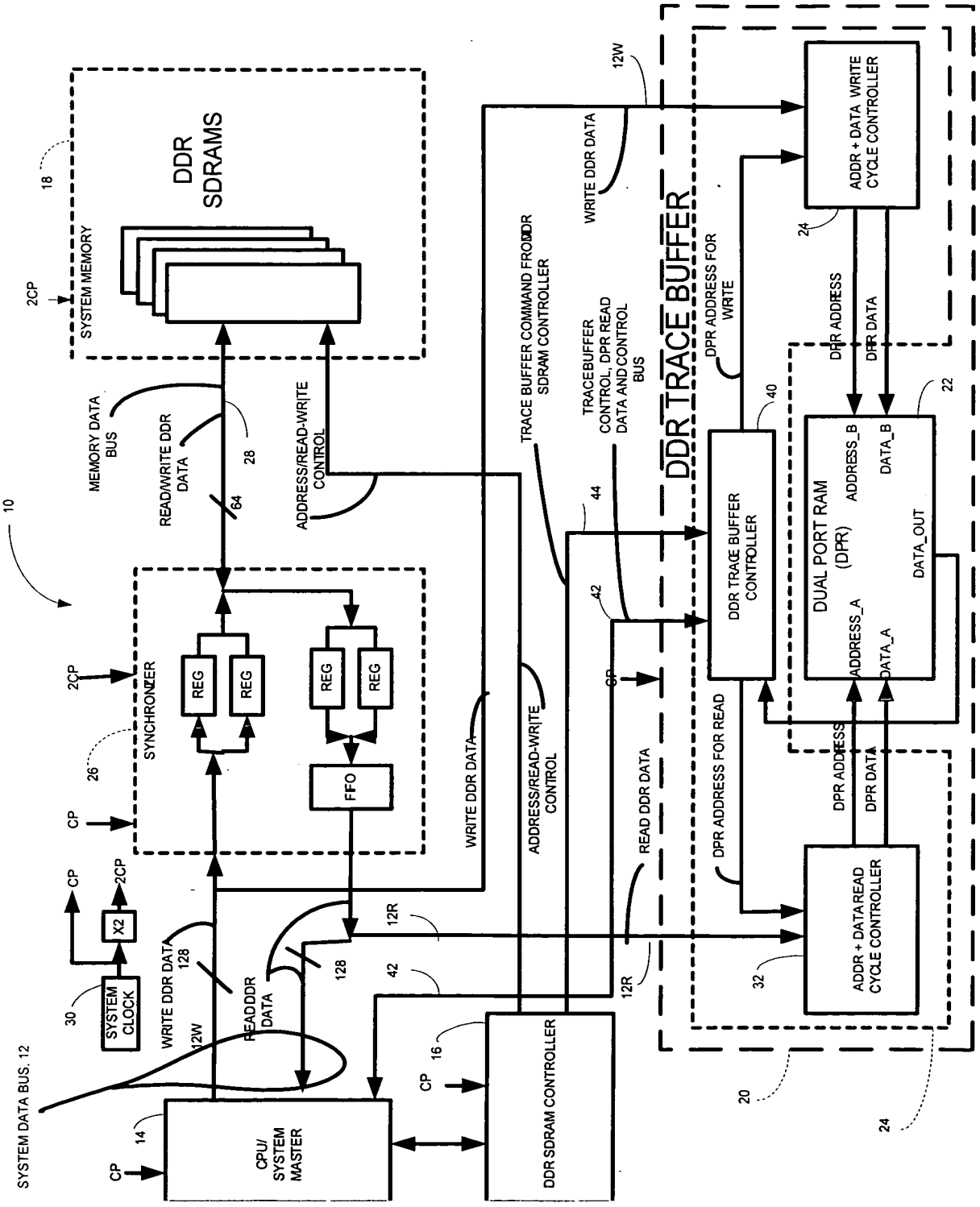
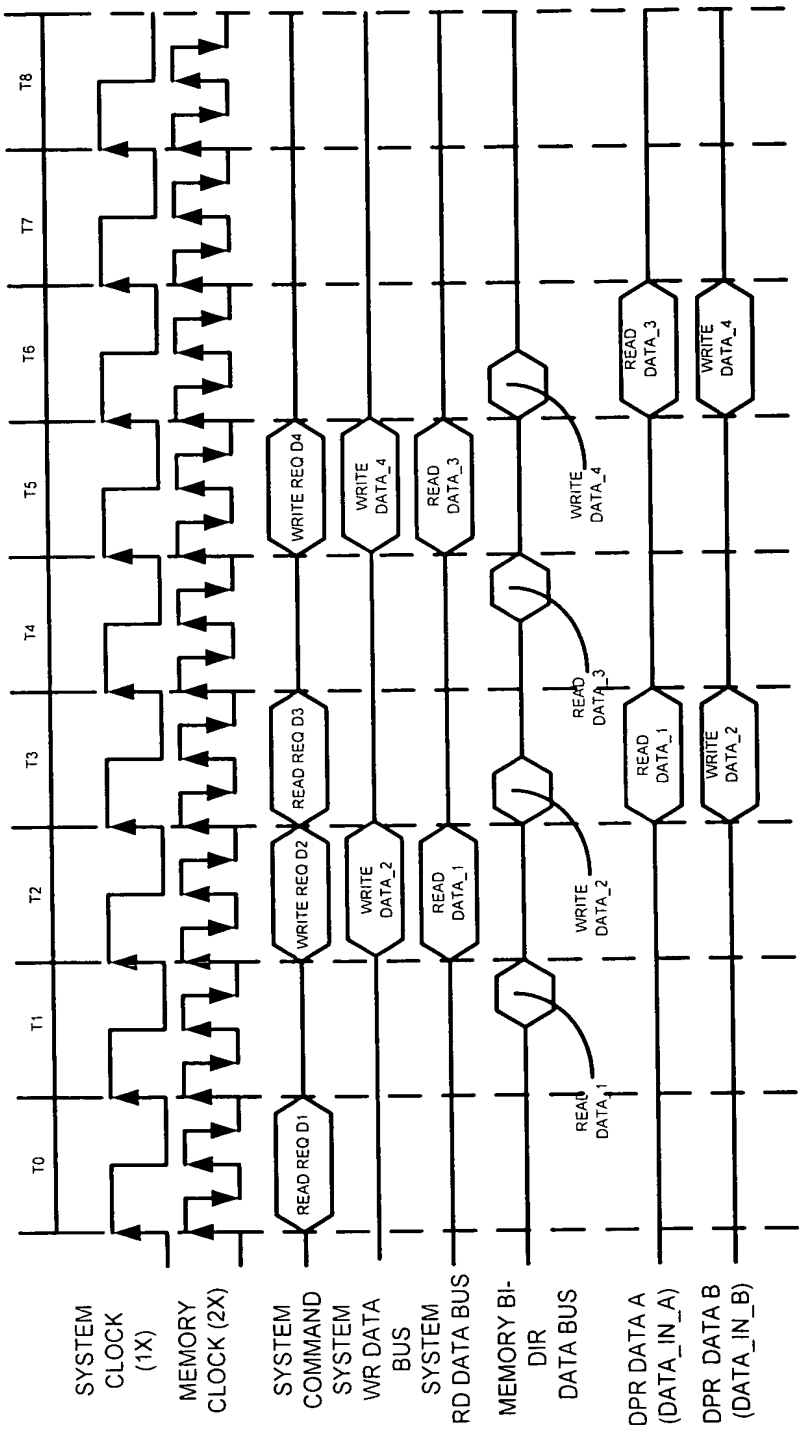

DDR SDRAMS
SYSTEM MEMORY
18
2CP
MEMORY DATA BUS
READ/WRITE DDR DATA
64
28
ADDRESS/READ-WRITE CONTROL
10
SYNCHRONIZER
26
REG
REG
REG
REG
FFO
CP
2CP
X2
SYSTEM CLOCK
30
WRITE DDR DATA
128
12W
READDDR DATA
128
12R
42
SYSTEM DATA BUS. 12
CPU/ SYSTEM MASTER
14
16
DDR SDRAM CONTROLLER
WRITE DDR DATA
ADDRESS/READ-WRITE CONTROL
TRACE BUFFER COMMAND FROM SDRAM CONTROLLER
TRACEBUFFER CONTROL, DPR READ DATA AND CONTROL BUS
44
READ DDR DATA
6P
DDR TRACE BUFFER
DDR TRACE BUFFER CONTROLLER
40
DPR ADDRESS FOR WRITE
DPR ADDRESS FOR READ
DUAL PORT RAM (DPR)
ADDRESS_A
DATA_A
ADDRESS_B
DATA_B
DATA_OUT
22
DPR ADDRESS
DPR DATA
ADDR + DATA WRITE CYCLE CONTROLLER
24
ADDR + DATA READ CYCLE CONTROLLER
32
20
24

FIG. 1



T0	- CPU REQUESTS READ 1
T1	- READ DATA_1 IS PUSHED ONTO MEMORY BUS BY DDR
T2	- CPU PERFORMS WRITE 2 - WRITE DATA_2 IS PUSHED ONTO SYSTEM BUS BY CPU - READ DATA_1 IS PUSHED ONTO SYSTEM BUS BY SYNCHRONIZER
T3	- CPU REQUESTS READ 3 - WRITE DATA_2 IS PUSHED ONTO MEMORY BUS BY SYNCHRONIZER - ADDR+DATA CTL FOR READ CYCLE WRITES DATA TO DPR - ADDR+DATA CTL FOR WRITE CYCLE WRITES DATA TO DPR
T4	- READ DATA_3 IS PUSHED ONTO MEMORY BUS BY DDR
T5	- CPU REQUESTS WRITE 4 - WRITE DATA_4 IS PUSHED ONTO SYSTEM BUS BY CPU - READ DATA_3 IS PUSHED ONTO SYSTEM BUS BY SYNCHRONIZER
T6	- WRITE DATA_4 IS PUSHED ONTO MEMORY BUS BY THE SYNCHRONIZER - ADDR+DATA CTL FOR READ CYCLE WRITES DATA TO DPR - ADDR+DATA CTL FOR WRITE CYCLE WRITES DATA TO DPR

FIG. 2

FIG. 3

DUAL PORT RAM
(DPR)

ADDRESS LOCATION	DATA
A_x	READ DATA_1
A_{x+1}	WRITE DATA_2
A_{x+2}	READ DATA_3
A_{x+3}	WRITE DATA_4